WE CLAIM:

1. A heterojunction bipolar transistor (HBT), comprising:

successive emitter, base and collector layers,

an InP sub-collector layer, and

a thermally conductive InGaAs contact layer between said collector and sub-collector layers.

2. The HBT of claim 1, said contact layer having a thickness not greater than about 500 Angstroms.

3. The HBT of claim 2, said contact having a thickness in the approximate range of 100-200 Angstroms.

4. The HBT of claim 1, wherein said contact and sub-collector layers extend lateral to said collector layer.

5. The HBT of claim 4, further comprising a contact pad on said contact layer lateral to said collector layer for establishing a contact to the collector layer through the contact and sub-collector layers.

6. The HBT of claim 1, wherein said sub-collector layer includes a functional portion aligned with said collector layer, and an electrically insulating portion lateral to said collector layer and outside the area of said functional sub-collector portion to electrically isolate said HBT.

7. The HBT of claim 6, wherein said sub-collector layer extends laterally beyond said contact layer, and said insulating portion of the sub-collector layer is lateral to said contact layer.

8. The HBT of claim 6, said insulating portion of the sub-collector layer including implanted ions and associated trapped conductors.

9. A double heterojunction bipolar transistor (DHBT), comprising;

an InP or InAlAs emitter,

an InGaAs base,

an InP collector,

an InP sub-collector, and

an InGaAs contact layer between said collector and sub-collector which establishes, together with the sub-collector, a low resistance contact to the collector, said contact layer being thin enough to provide a substantially higher thermal conduction path between said collector and sub-collector than would bulk InGaAs.

10. The DHBT of claim 9, said contact layer having a thickness not greater than about 500 Angstroms.

11. The DHBT of claim 10, said contact layer having a thickness in the approximate range of 100-200 Angstroms.

12. The DHBT of claim 9, wherein said contact layer in doped N+.

13. The DHBT of claim 9, wherein said contact layer and sub-collector extend lateral to said collector.

14. The DHBT of claim 13, further comprising a contact pad on said contact layer lateral to said collector.

15. The DHBT of claim 13, wherein at least a portion of said sub-collector lateral to said collector is electrically insulating to electrically isolate said HBT.

16. The DHBT of claim 15, wherein said sub-collector extends laterally beyond said contact layer, and said insulating portion of the sub-collector is lateral to said contact layer.

17. The DHBT of claim 15, said insulating portion of the sub-collector including implanted ions and associated trapped conductors.

18. A heterojunction bipolar transistor (HBT), comprising:

successive emitter, base and collector layers, and

an InP sub-collector layer having an electrically insulative portion which electrically isolates the HBT.

19. The HBT of claim 18, wherein said sub-collector layer extends laterally beyond said collector layer, with said insulative portion located lateral to said collector layer.

20. The HBT of claim 18, wherein said insulative portion of the sub-collector layer includes implanted ions and associated trapped conductors.

21. The HBT of claim 18, wherein said ions have a more uniform than Gaussian distribution through the thickness of said sub-collector layer.

22. A method of fabricating a heterojunction bipolar transistor, comprising:

forming in succession an InP sub-collector layer, a thin electrically conductive InGaAs contact layer, and collector, base and emitter layers on a substrate, and

etching said collector, base and emitter layers to a desired shape, using said contact layer as an etch stop to protect said sub-collector layer when the collector layer is etched.

23. The method of claim 22, further comprising the step of etching at least a portion of said contact layer lateral to said collector layer after etching said collector, base and emitter layers.

24. The method of claim 23, wherein said contact layer is etched only lateral to a lateral margin adjacent said collector layer.

25. The method of claim 24, further comprising the step of forming a contact pad on said contact layer in said margin.

26. The method of claim 22, wherein said contact layer is formed with a thickness not greater than about 500 Angstroms.

27. The method of claim 26, wherein said contact layer is formed with a thickness in the approximate range of 100-200 Angstroms.

28. A method of electrically isolating a bipolar transistor, comprising:

forming said transistor with an InP sub-collector, and

rendering a portion of said sub-collector electrically insulative to electrically isolate the transistor.

29. The method of claim 28, wherein said electrically insulative portion is established by implanting ions into said sub-collector to trap conductors in the insulative portion.

30. The method of claim 29, wherein said ions are implanted into the sub-collector lateral to the remainder of the transistor.

31. The method of claim 29, wherein said ions are implanted into the sub-collector in multiple implants at different respective principal implant depths to obtain a more uniform ion distribution than that resulting from a single implant.

32. The method of claim 28, said transistor comprising a heterojunction bipolar transistor (HBT).